DOPPLER ULTRASONIC SYSTEM FOR FLOW MEASUREMENT IN PATIENTS WITH DIABETIC FOOT USING RECONFIGURABLE LOGIC AND WISHBONE ARCHITECTURE

SISTEMA ULTRASÓNICO DOPPLER PARA LA MEDICIÓN DE FLUJO EN PACIENTES CON PIE DIABÉTICO MEDIANTE EL EMPLEO DE LÓGICA RECONFIGURABLE Y ARQUITECTURA WISHBONE

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Recibido 28/3/2016; Aceptado 22/7/2016

The first results in the design of a pulsed Doppler ultrasound system are presented, which aims to detect alterations of diabetic foot cataloged as ”high risk”, associated with the processes that lead to occlusion of blood vessels. Therefore, measurement of blood flow gives the level of damage in the affected area and the state of the blood vessels, constituting a noninvasive diagnostic test. The system was designed from the classical conceptions of Pulsed Doppler systems and also, incorporates advanced digital design techniques based on hybrid hardware-software implementations (FPGA) on reconfigurable platforms. The analog system architecture is shown and finally, its most outstanding features and the expected results of the design are exposed.

Se presentan los primeros resultados en el diseño de un sistema ultrasónico Doppler Pulsado, que tiene como objetivo detectar alteraciones que cataloguen al pie diabético como de “alto riesgo”, vinculadas con los procesos que provocan la oclusión de los vasos sanguíneos. Por tanto, la medición del flujo sanguíneo proporciona el nivel de afectación del área dañada y el estado de los vasos sanguíneos, constituyendo una prueba diagnóstica no invasiva. El sistema se diseñó partiendo de las concepciones clásicas de los sistemas Doppler Pulsados y además, incorpora técnicas avanzadas de diseño digital basadas en implementaciones híbridas hardware-software (FPGA), sobre plataformas reconfigurables. Se muestra la arquitectura analógica del sistema, se dan sus características más sobresalientes y finalmente, se exponen los resultados esperados de dicho diseño.

PACS: pulsed Doppler ultrasonic system, 43.35.Zc, 81.70.Cv. blood vessels occlusion, 43.35.Wa. hardware-software hybrid implementations, 84.40.Lj. reconfigurable platforms 84.40.Lj

I. INTRODUCTION

The Vascular Doppler Ultrasound (VDU) is an advanced, non-invasive technique that not only provides information on the human vascular structure, but is also able to measure blood flow in various parts of the circulatory system related to serious diseases, such as the so called Diabetic Foot. It also helps to determine the resistance of the blood vessels to blood flow, and provides relevant information on the state of them by means of ultrasound, using an ultrasonic sensor which is aligned with the artery or vein to be measured. It constitutes a diagnostic test which evaluates the intensity of blood flow, employing the Doppler effect produced during interaction with the red blood cells. Among the applications of this technique are:

- Decide whether the treatment should be surgical or with drugs.
- Diagnosing thrombosis in the venous system of the legs.
- Checking obstructions in arteries of the neck (carotid) and arteries in legs and arms.

Doppler measurement systems used in medicine can be continuous or pulsed type. The continuous system transmits a continuous ultrasound beam such that the transmission and reception of ultrasound occurs simultaneously in the transducer, which makes it impossible to determine the depth at which the Doppler effect occurs [1, 2].

In pulsed systems, a pulse train of short duration is transmitted and received, getting information before transmitting the next pulse train. The main advantage between pulsed Doppler and continuous Doppler consists in obtaining information about the distance to the object being surveyed (the time interval between transmission and reception can be converted into a distance, knowing the speed of ultrasound in the medium in question). It is most often used today for this type of equipment.

The pulsed Doppler systems require of some circuits to enable that signals be transmitted and received at appropriate times and to sample and store the demodulated signals. The ultrasonic transducers used in pulsed units have one piezoelectric element for transmitting and receiving ultrasound [4–6].

This paper describes a system for measuring blood flow by Doppler technique in patients with Diabetic Foot and to make it happen, it is necessary to know the permeability of the blood flow, which is determined by measuring systolic blood pressure (PAS) in arms and ankles. For it, the information from Doppler measurements done in arteries located in the same place is employed.

II. DETERMINATION OF SYSTOLIC BLOOD PRESSURE (PAS)

The permeability of the blood circulation can be obtained by determining systolic blood pressure (PAS) in arms and ankles using a blood pressure cuff and a Doppler equipment. PAS will be measured in both arms and close by the ankles by which the value of ankle brachial index can be obtained.

The procedure is shown below:

1. Maintain the patient at rest for 5 minutes.
2. The measurement is made using the Doppler transducer at an angle of 60° respect to the artery to be measured: the elbow's humeral, in the pedal and the foot posterior tibia.
3. The blood pressure cuff should be inflated to at least 20 *mm Hg*, in order to obstruct the conduit and then deflated gently (−2 *mm Hg/sec*) to ensure greater accuracy.
4. Then during deflation, the PAS will be obtained at the time the appearance of the Doppler arterial pulsation is detected.
5. PAS is calculated using the Doppler transducer supported in both brachial arteries (above the elbow) and in pedis and posterior tibial arteries. In both cases, the highest reading values of pressure are selected to calculate the PAS.
6. Then, to obtain the ankle/brachial index (ITB), the highest value of PAS obtained in the ankle is divided by the highest value of PAS obtained in arm:

$$ITB = \frac{Ankle\ Pressure}{Arm\ Pressure} \tag{1}$$

Arterial insufficiency depending on the ITB isshown in Table 1.

III. SYSTEM DESCRIPTION

The system consists of an 8 MHz ultrasonic Doppler sensor, an analog module, a digital module and a PC. The analog module and the sensor are responsible for the acquisition and pre-processing of the Doppler signal from the measurement made on a blood vessel. The digital module generates the control signals used by the analog module, processes the signal from this module and sends it to a PC via USB port using FPGA technology. The PC is responsible for receiving the sent signals, process them and finally show the deployment in the display, see Figure 1.

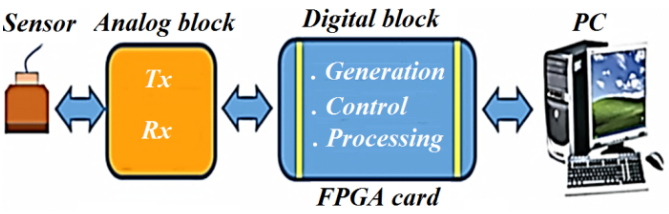

Figure 1. Block diagram of the ultrasonic Doppler system.

Table 1. Arterial Insufficiency

T/B	Disturbance
> 0.5	Severe Vascular Disease
0.5 – 0.8	Moderate Vascular Disease
< 0.9	Suspected Vascular Disease
0.9 – 1.3	Acceptable Range

III.1. Doppler ultrasonic sensor

The ultrasonic sensor is responsible for emit an 8 *MHz* pulse train to the vascular tissue and then receive echoes containing information from Doppler ultrasound, produced in blood coursing through a vessel, see figure 2. The 8 *MHz* piezoelectric element has two wire welded on its sides and is adequately glued onto one surface of a piece made of rexolite material, which was previously acoustically designed. The wires are welded to a shielded cable having a connector at its other end.

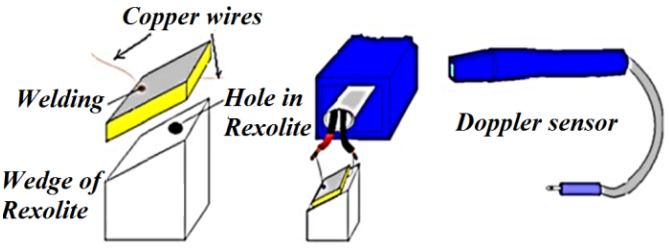

Figure 2. Construction of Doppler ultrasonic sensor.

III.2. Doppler analog module

The analog Doppler module is shown in figure 3 as part of the system and is highlighted with dashed lines. It consists of four main sections: a transmitter, a receiver, two modulators and two bandpass filters. It operates under the known Pulse-echo principle. The transmitting section drives the 8 *MHz* sensor by means of a pulse train of the same frequency. As a result, the transducer emits an ultrasonic train of the same frequency which interacts with the blood flow through a vessel, corresponding to an artery or a vein, which causes that a Doppler signal be received and amplified by the receiver.

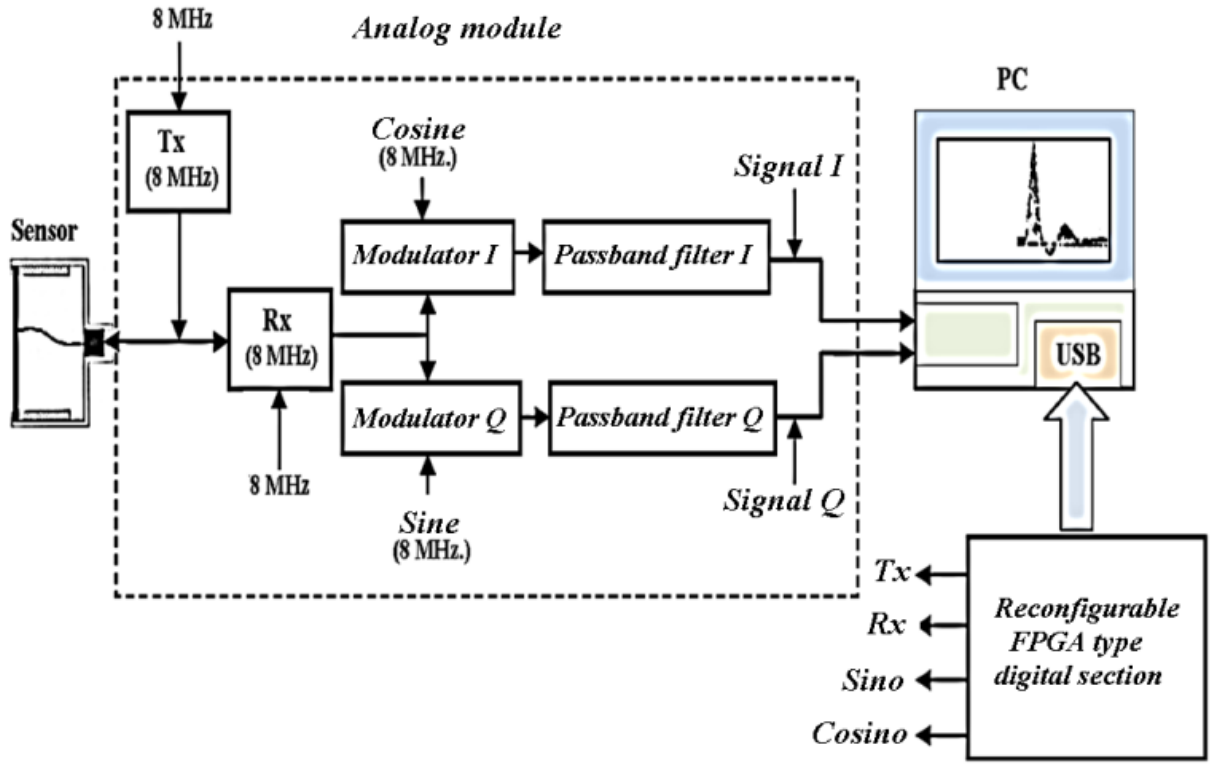

Figure 3. Ultrasonic Doppler system handled by FPGA.

The receiver, connected to the transmitter output, is formed by a tuned input stage and an amplifier stage implemented with a FET transistor. It has a voltage gain of 9.5 *d*B, wide bandwidth and its output signal is applied to two modulators. The modulators, implemented from a transistor stage have 3 main functions: coupling with the previous stage, mixer and audio amplifier with low pass response. The modulators receive at their emitter inputs the Doppler signal from the receiver, and the base inputs, receive two 8 *MHz* signals from the digital module, which are shifted 90 degrees and thus is possible to obtain a phase quadrature modulation. The outputs of the modulators are low-pass filtered with cutoff frequencies of 3.3 *kHz* and a slope of −6 *dB/oct*., so that, the difference between the input signals is obtained at the output of the modulators.

Finally, these signals at the outputs of the modulators are filtered again by bandpass filters, with cutoff frequencies of 330 Hz and 8 *kHz* and slopes of 18 *dB/oct* and −30 *dB/oct*, respectively, obtaining finally the known signals *Q* and *I*, which will be processed in the digital section.

III.3. Digital module to control and processing

The analog module is controlled by a digital module which consists of programmable and reconfigurable FPGA elements, where the corresponding signals for the operation of the analog module are produced, together with the signals that interface with the PC. The LabView program is employed in the PC to process conveniently the signals acquired from the FPGA, which are shown later in its display.

Wishbone architecture

Digital module implementation is based on the wishbone architecture, developed as an open code computer bus allowing communication among the parts of an integrated circuit, intended to be a logical bus. Its specification is not related to electrical information or a bus topology. It is written in terms of signals, clock cycles or high and low levels. Furthermore, it consists of a specification of openness that allows the user to configure the system based on a predefined set of permissions and prohibitions, see figure 4.

This ambiguity is deliberate as Wishbone is designed to allow designers to combine many designs described in Verilog, VHDL or other logical description languages for EDA. The bus provides a standard way of combining different hardware designs as cores. It fits common bus topologies such as point to point, many to many, hierarchical or switched fabric.

The bus is defined to allow structures of 8, 16, 32 and 64 bits. All the signals are synchronized to the same clock, but the responses of the slaves must be generated in combinational form for maximum performance. It also allows the addition of a tag bus to describe the data.

Wishbone implementation

The digital module was implemented in a Spartan 6 Xilinx FPGA development platform, taking into account its great

functional and reconfigurable advantages. Such a device was used to implement the generation of all control signals: the synchronism and the acquisition of signals by the A/D converter (located in the analog module), to do the processing of Doppler signals (acquired by said A/D converter) and finally, to send such signals to the computer through the USB port.

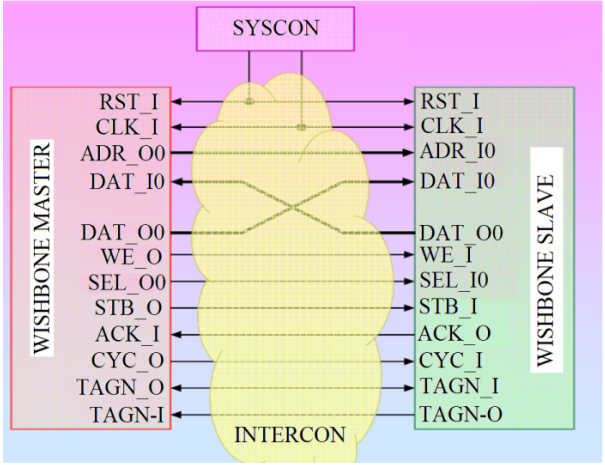

Figure 4. Master-slave Wishbone interface.

To do this, it was used the hardware description language (VHDL) and the Wishbone interface, taking into account their functional and great reconfigurable advantages. These signals were programed in XILINX ISE 13.1 platform.

Input register of generating control signals module

- *value_ent:* It allows selecting the system working frequencies of 6 and 8 *MHz*.
- *pulses_number:* It allows the choice and to vary the number of pulses that integrate the signals in phase and in opposite phase to the transmission process.
- *prf_selection:* It allows the choice and variation of the system repetition frequency.
- *ffmuestreo:* It enables to change the sampling rate of the acquisition system.
- *d_delay:* It selects the start of acquisition of the A/D converter.

Control signals generated at the output

To implement the output signals, the control signals generation module was created(Unit_tubes_controller) and implemented in VHDL language, which describes the operation of real electronic devices by means of software. These signals will be responsible for controlling the analog transmitter described above.

Enable signal of ultrasonic transmitter

This signal supplies logic 1 for a given time, allowing the activation of the ultrasonic transmitter belonging to analog module, see Figure 5.

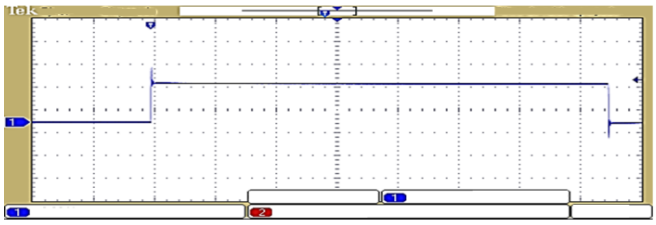

Figure 5. Enable signal of ultrasonic transmitter.

Burst OUT signal to the pulsed Doppler

To obtain the Burst OUT signal, the previously selected frequency of 8 *MHz* is employed. Initially, the number of pulses of this signal is selected and the value of the repetition frequency is generated.

To generate this signal, the arch_divider_core architecture is used, which is nothing more than a fixed 8 bit counter, where cnt_clock and cnt_countcnt_reset variables are used.

As a result, a fixed repetition frequency in the system is obtained by means of the default value of the variable cnt_count. This means that the system will always have a fixed repetition rate between burst and burst, previously generated.

Then, by means of the architecture_arch_counter_core program, and through 16-bit_cnt_count variable, a higher value counter in correspondence with the first counter is achieved, offering the possibility of increasing the repetition frequency. This 16-bit_cnt_count value can also be prefixed or selected by the user from a personal computer. In figure 6, the pulsed signal which is applied to the transmitter is shown, where the number of pulses and the repetition frequency were previously selected.

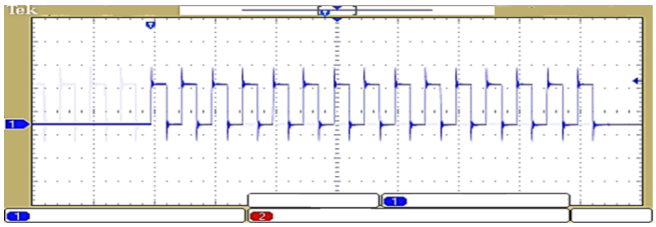

Figure 6. Transmitting 8 *MHz* pulsed Doppler signal.

Reception_gate signal

This signal is responsible for enabling the receiver during transmission, protecting its first stage from the high voltage. If the transmission mode is continuous, the protection is not required because the transmission occurs with low voltage, see figure 7.

Generated sine and cosine signals

Two 8 *MHz* signals shifted 90 degrees from each other (sine and cosine), being in phase quadrature, are applied to modulators in the analog module (see figure 8). Then,

they are mixed with the received Doppler signal, occurring a phase quadrature modulation.

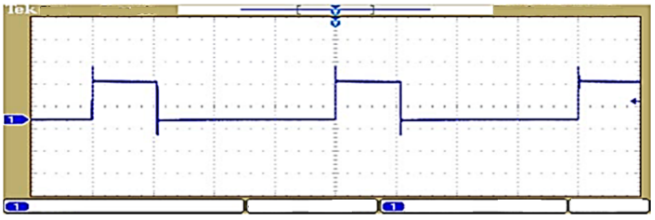

Figure 7. Gate 8 *MHz* pulsed signal.

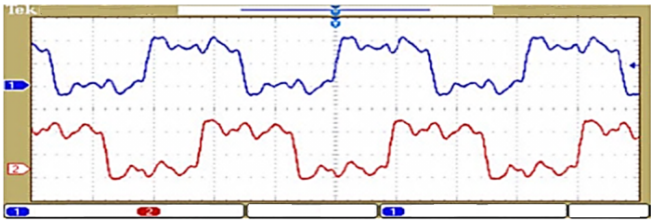

Figure 8. 8 *MHz* phase quadrature signals.

The signals obtained at the output of the two modulators are fed into low pass filters, located in the analog module, with cutoff frequencies of 7 *kHz* and slope of –30 *dB/oct*. The filtered signals, corresponding to the difference between the Doppler signal and the modulating quadrature signals, are in the audible range, known as *I* and *Q* signals.

Wishbone communication module

This module is responsible for interconnecting all input and output signals between the Wishbone module and different implemented modules, both for generation and for signal acquisition, see Figure 9. This stage was programmed so that the system starts with default values, that means, when executed, the system pre-sets the values in the main program.

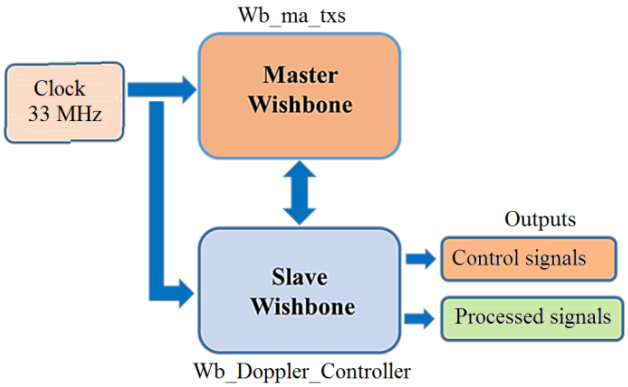

Figure 9. Wishbone implementation.

Subsequently, to run properly the Wishbone interface provides the possibility to change the values of frequency, number of pulses and frequency of repetition, as desired by the user, using a "case" function, programmed into the FPGA. All these changes are executed in real time by a program in a microcomputer (Labview), via the USB port. For this, by means of the program edit, the user can change the desired values at all times.

Signal acquisition module

It is the system acquisition module that drives an A/D converter and is conceived by means of the development of a state machine, which will be in charge of controlling the entire conversion process of the I and Q Doppler signals (conversion in parallel), see figure 10.

Ensures the following aspects:

- The A/D converter clock signal is in high level "1".
- The initial values are defined for the converter: CNVST is at high level "1" (start conversion).
- The OB_2C signal is prefixed to "1" (define the output signal as binary).
- The Byteswap signal is preset to "1" (selects the A/D converter be 16 Bit in its output).
- The Busy signal in low level "0" (output signal which indicates the device is ready for conversion).

Then, in the next cycle, the CNVST signal takes a low value for a time of 5 *ns*, telling the A/D that conversion will start. When it begins, the Busy signal changes from logic "0" to "1", remaining this value until the completion of the conversion and the change to its previous state of "0", indicates that the data is ready to be acquired. The acquired data (1024 data) is stored in a 16 bit FIFO memory.

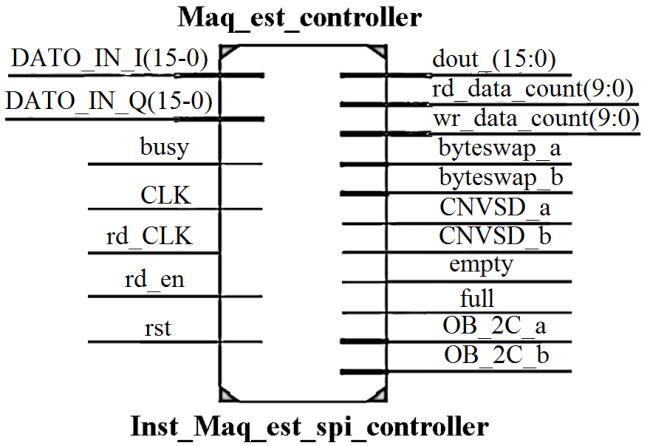

Figure 10. Design of the state machine in the FPGA.

The dram_full ≤ "1" instruction indicates whether the memory is filled and its contain can be sent via USB, (the 1024 byte of data to be processed and then displayed on a personal computer), see figure 11.

USBS6 CESYS module and used FPGA card

This is the FPGA module used in the design with their proper benefits: great number of system channels, a powerful FPGA, higher working frequency, more input-output connectors

and it has a USB port.

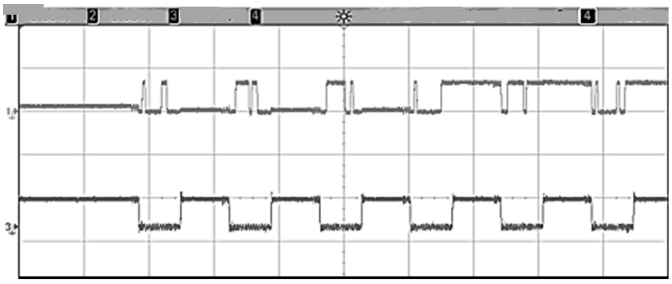

Figure 11. Real time acquisition diagram of AD converter.

Main Characteristics

- XILINX SPARTAN-6TM XC6SLX16-2CSG324C FPGA device.
- USB2.0 CYPRESSTM CY7C68013A controller.
- FPGA configuration using USB2.0, JTAG or SPI-Flash.
- Memory: 16Mb SPI-Flash Numonyx M25P16, 128Mb Quad-SPI-Flash Macronix MX25L12845EMI-10G, 1Gb low-power DDR SDRAM Micron, Technology MT46H64M16LFCK-5.
- Expansion connector, (2x25-Pin standard RM2.54mm header, VG 96-pin connector).
- 48 *MHz* system clock with external clock option.
- Can be programmed using C++ o VHDL.
- Peripherals: USB to serial UART FTDI FT232R, HEX rotary DIP switch, 3 status.

IV. IMPLEMENTATION OF SOFTWARE DESIGNED IN LABVIEW

In order to view and control the signals coming from the receiver, these are A/D converted and posteriori processed in the FPGA, where the data is sent via USB to a personal computer that runs LabView. Figure 12 shows the front panel which is the screen where the Doppler signals are displayed in real time and the flow value through the vessel [5].

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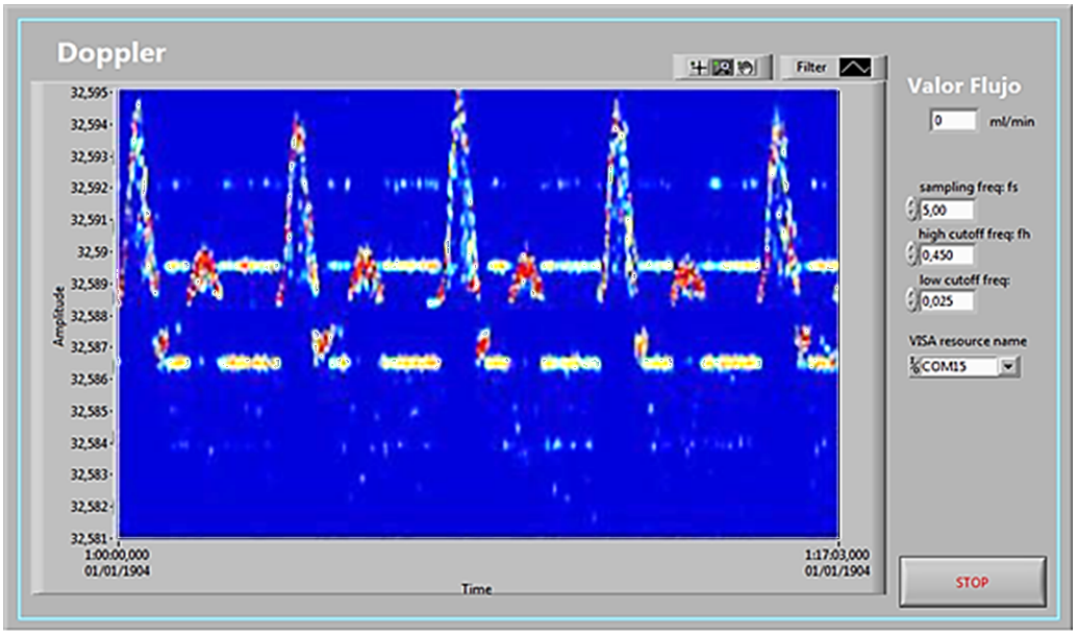

Figure 12. Frontal panel of Doppler system.